

**Notice of References Cited**

Application/Control No.

09/955,926

Applicant(s)/Patent Under  
Reexamination  
MALLARDEAU ET AL.

Examiner

Thomas J. Magee

Art Unit

2811

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,492,241 B1	12-2002	Howard E. Rhodes et al.	438/386
	B	US-6,358,820 B1	03-2002	Shigenobu Maeda	438/459
	C	US-6,133,599	10-2000	Jan Mye Sung et al.	257/296
	D	US-6,294,464 B1	09-2001	Jigish D. Trivedi	
	E	US-			
	F	US-			
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	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Syd. R. Wilson, Clarence J. Tracy, and John L. Freeman, Jr., "Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey (1993), pp. 82-84, 157, 868.
	V	S. Wolf, "Silicon Processing for the VLSI Era: Volume 2 - Process Integration," Lattice Press, Sunset Beach, CA (1990), pp. 12-13.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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